Production Test Consideration for Mixed-Signal IC with Background Calibration

Takuya YAGI, Haruo KOBAYASHI, Hiroyuki MIYAJIMA, Youhei TAN
Satoshi ITO, Satoshi UEMORI, Nobukazu TAKAI, Takahiro J. YAMAGUCHI
Electronic Engineering Department, Graduate School of Engineering, Gunma University, Kiryu, 376-8515, Japan
phone: 81-277-30-1788 fax: 81-277-30-1707 email: k_haruo@el.gunma-u.ac.jp

Abstract— **This paper proposes an improved method of background calibration that reduces production testing time of mixed-signal ICs. Production testing time typically consists of "calibration convergence time" + "functional testing time after calibration convergence". The method that is proposed here reduces average calibration convergence time. This method does not require extra ADC operation for functional testing after calibration convergence, and can be implemented with little additional on-chip test-support circuitry when testing is performed by ATE (Automatic Test Equipment). As an application of this method, we discuss background calibration of pipelined ADCs and present simulation results that demonstrate its effectiveness in reducing testing time.**

Keywords : Analog BIST, ATE, Background Calibration, Mixed-Signal IC Test, Digitally-Assisted Analog Technology

I. Introduction

Production testing analog circuitry in mixed-signal SoC is currently an important issue in the semiconductor industry; testing time must be reduced, by improving the testability, to reduce testing costs [1] - [12].

This paper discusses methods of reducing the testing time of digitally-assisted analog circuits [14] in mixed-signal SoC. Digitally-assisted analog circuit design is very important in this nano CMOS era – however, only a few papers have discussed testing of such circuits [11], [12], so we approach this issue in this paper.

If the analog part is designed to be calibrated in the background, its testing time typically consists of calibration convergence time plus testing time after calibration convergence. Background calibration time can be very long in many cases.

We here propose a method of reducing average calibration convergence time during testing. This method does not require extra ADC operation for functional testing after calibration convergence, and – when using ATE (Automatic Test Equipment) for testing – can be implemented with a little additional on-chip memory read/write circuitry. We consider the application of this method to the background calibration of a pipelined ADC using an open-loop residue amplifier [13], and we used MATLAB simulation to demonstrate its effectiveness in reducing testing time.

II. Proposed Method for Reducing Calibration Time

A. Basic Principle of Proposed Method

Fig.1 shows a block diagram of a typical pipelined ADC with background calibration. There are nonidealities in the feedback DAC and residue amplifiers of internal circuits such as the backend ADC and frontend ADC; digital calibration logic determines the correct ADC output using an Least-Mean-Squares (LMS) algorithm. The coefficient data (stored in memory) are continuously updated until the LMS algorithm converges (i.e. the coefficient data converge). After the calibration converges, the ADC output is digitally corrected using the coefficient data in the memory.

We consider here that *systematic* nonidealities, such as the residue amplifier nonlinearity, would correlate with each other among chips within the same wafer. Then values of the final convergence coefficient data in the memory would be similar among chips within the same wafer (or within the same lot); thus if the converged coefficient data in the memory of one chip (chip 1) is used as the initial coefficient data for another chip (chip 2), the calibration of chip 2 converges quickly.

To realize this scheme, we just need to modify the associated circuits by adding memory that stores calibration coefficient data – so that an external ATE can read and write the data during testing (Fig.2).

If the coefficient values in chip 1 converge to some values and they are stored in the memory, then the ATE reads the data from the memory and loads them into the memory of chip 2 as initial values, then testing of chip 2 starts (Fig.3). If chips 1 and 2 have similar process characteristics, then both calibration convergence data will be similar, and calibration of chip 2 will finish in a short time,

Similarly, the ATE loads the same initial data values into the memory for chip 3, chip 4, .. just before their testing starts; and their testing time is also reduced.

In practice, many chips are tested simultaneously, in parallel, and in this case the same initial data are stored in the memories of all the ADCs under test.

B. Case Study

Fig.4 shows a block diagram of a pipelined ADC with an open-loop residue amplifier where its nonlinearity (Fig.5) is calibrated in background. Fig.6 shows the ADC plus our proposed on-chip test-assist circuitry.

MATLAB simulation comparison for the pipelined ADC based on [13] between the proposed and conventional methods is shown in Figs. 7 and 8; Fig.7 shows the effective number of bits (ENOB) versus the iteration number while Fig.8 shows P1, P2, P3 parameters versus the iteration number, and we see that they average converge quickly with the proposed method. Fig.10 is another simulation results; it shows the histogram of the chips with respect to the number of the iterations for convergence (the total number of the chips is 1,024), and we see that the convergence time is less than half when the proposed method is used.

We also note that not only parameters p_1, p_2, p_3, but also parameters μ_1, μ_2, μ_3 in Fig.6 can be taken care of with our proposed method.

III. Proposed Method for Parallel Processing

Typically [11] the testing time of mixed-signal SoC consists of "calibration convergence time" plus "functional testing time after convergence". In this section we propose that the ATE performs functional testing for one chip and calibration for another chip in a parallel (pipelined) manner to reduce testing time (Fig.9).

The ADC with background calibration can output the corrected data after calibration convergence, and if we test it directly, first the ATE waits for convergence and then performs function testing. However, if the ATE can read the frontend ADC and backend ADC (uncorrected raw) data into buffer memory directly during calibration, it can reconstruct their correct data from the converged coefficient data. We propose here the following:

1) During chip 1 testing, the calibration of chip 1 is performed, and also the ATE downloads the frontend and backend ADC (uncorrected, raw) output data into its buffer memory.
2) After a while, the calibration of chip 1 converges, and the ATE downloads the converged coefficient data.
3) The ATE can reconstruct the correct ADC data from the uncorrected (raw) ADC data and the converged coefficient data, and also calculate its linearity and SNDR and so on, using its powerful DSP capability.
4) For chip 2 testing, the above procedure is repeated.

We consider that procedure 3) (calculation of correct ADC data in chip 1) and procedure 1) for chip 2 (calibration of chip 2) can be performed in parallel in the ATE; when calibration time and functional tesing time are comparable, the functional testing time of chip 1 is effectively hidden, and ADC testing time is reduced.

In order to realize the above scheme, we just need to add circuits so that the ATE can read the frontend and backend ADC data directly.

IV. Conclusions

This paper has proposed testing time reduction methods for mixed-signal SoC with background calibration.

1) The circuit characteristics among chips within the same wafer (or the same lot) show some correlation, and we propose to use the converged calibration coefficient data of one chip as the initial data for other chips; the calibration time (i.e., testing time) of "other chips" is thus reduced.
2) We propose the method that enables an ATE to perform functional testing of one chip and time-consuming calibration of another chip in a parallel (or pipelined) manner in order to reduce testing time. Powerful DSP capability in the ATE would enable this scheme.

Digitally-assisted analog techniques (such as digital background calibration) are becoming more popular in this nano CMOS era [14], and we believe that testing methods are also very important.

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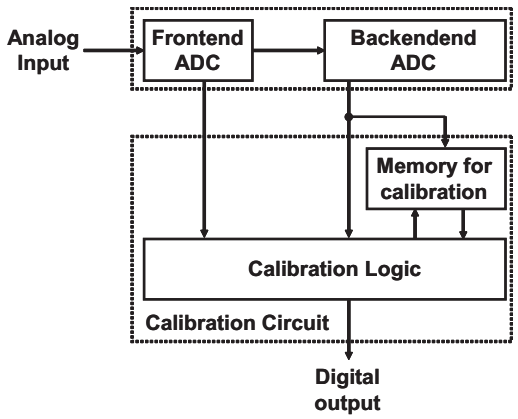

Fig. 1. Block diagram of a typical pipelined ADC with background calibration.

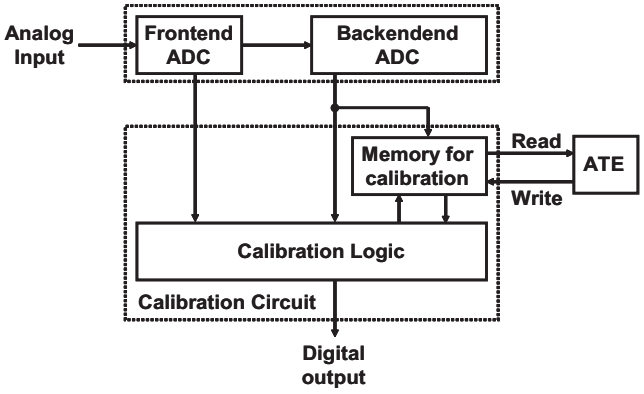

Fig. 2. Block diagram of a typical pipelined ADC with background calibration and memory read/write circuit.

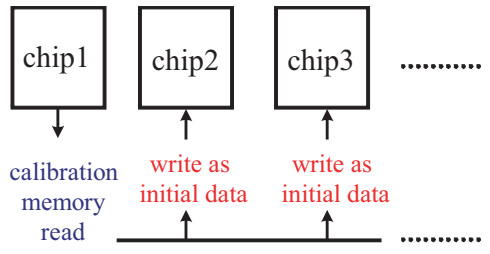

Fig. 3. Explanation of the proposed method for fast calibration convergence. The ATE reads the converged data from chip 1 memory and downloads it to chip 2, 3, 4, ... as initial data.

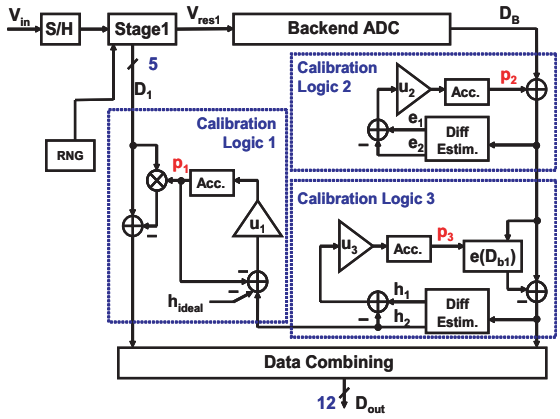

Fig. 4. Block diagram of the pipelined ADC with background calibration logic in [13].

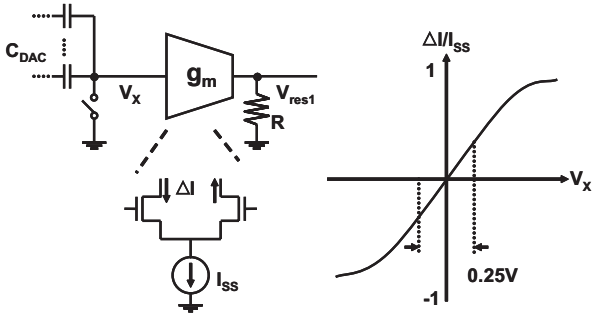

Fig. 5. Open-loop residue amplifier with nonlinearity used at the end of "Stage 1" in Fig.4.

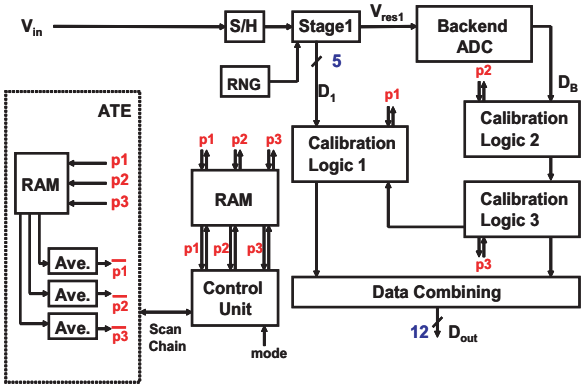

Fig. 6. Block diagram of the pipelined ADC with background calibration logic in [13], plus our proposed on-chip test-assist logic.

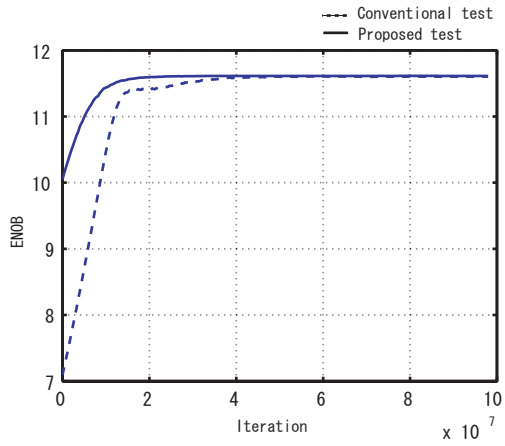

Fig. 7. MATLAB simulation results of the proposed method. ADC ENOB (effective number of bits) converges quickly when the proposed method is applied.

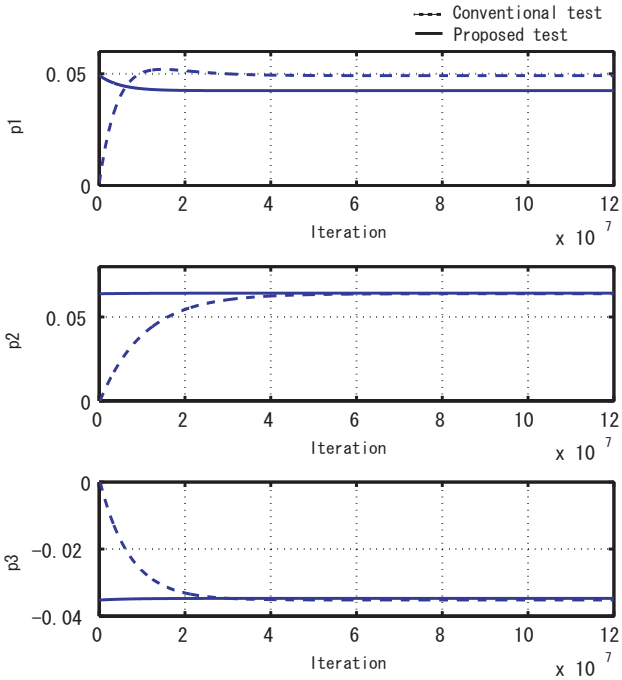

Fig. 8. MATLAB simulation results of the proposed method. Parameters P1, P2, P3 converge quickly when the proposed method is applied.

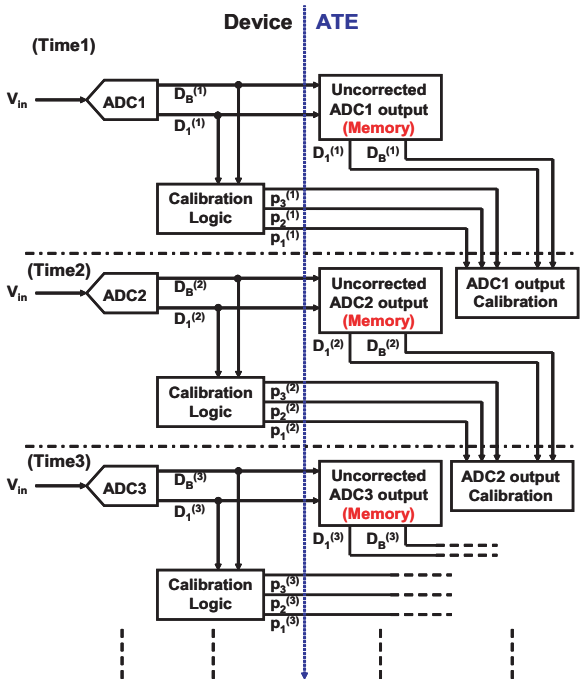

Fig. 9. Proposed method where the calibration and function test are performed in pipelined manner.

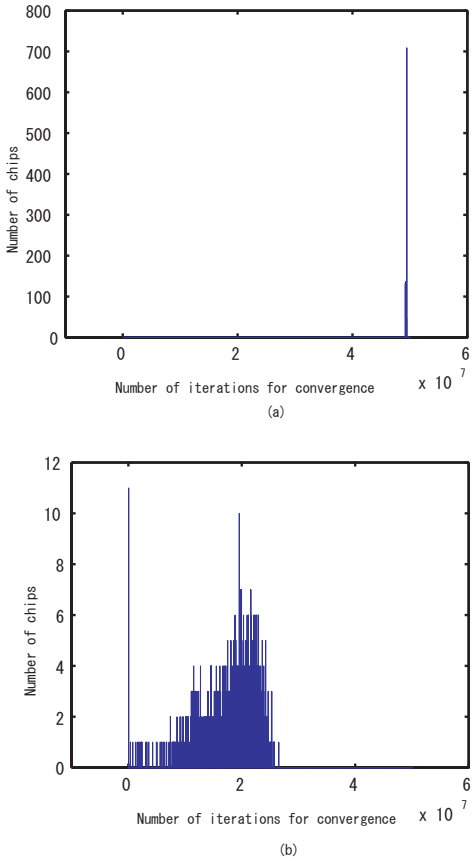

Fig. 10. Simulation result comparison of convergence time between the proposed and conventional methods. (a) Comventional method. (b) Proposed method.